## REMARKS

The Applicant has filed the present Response in reply to the outstanding Final Rejection of November 18, 2002 and the Applicant respectfully submits that the Response is fully responsive to the Final Rejection for reasons set forth below.

In the Final Rejection, the Examiner finally rejected Claims 1-21 pursuant to 35 U.S.C. §102(b), as allegedly anticipated by Katata, *et al.* (U.S. Patent No. 5,631,644) (hereinafter "Katata"). More specifically, in response to the Applicant's arguments in the Amendment of August 21, 2002, in which the Applicant argued that Katata does not disclose "adjusting the quantization step size ... [based on] a bit balance of the generated bit count with respect to the to the average bit rate," the Examiner alleged that Katata at the cited passages discloses "adjusting the quantization step size based on the generated the bit rate and average bit rate with respect to buffer occupation."

In traversing the rejection of independent Claims 1, 11 and 21 pursuant to 35 U.S.C. §102(b), the Applicant respectfully submits that Katata does not disclose adjusting the quantization step size for each second image unit based on the bit balance of the generated code bit count with respect to the average code bit rate, as particularly recited in Claims 1, 11 and 21. The Applicant disagrees with the Examiner's allegations and characterizations of the present invention in the response to arguments section of the Final Rejection for the following reasons. The Examiner characterized the present invention, as a whole, being directed to quantization step size adjustment based on the generated bit rate with respect to the average bit rate and buffer occupation. However, the recited quantization step size adjustment is rather based on the **bit balance** of the



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generated code bit count with respect to the average code bit rate, as recited in the Claims 1, 11 and 21. To the contrary of the present invention as claimed, the Applicant respectfully submits that Katata's quantization step size adjustment does not disclose this feature. More specifically, Katata discloses that its quantization step size determining circuit 65 calculates a virtual buffer fullness (dj) based on a generated code quantity (B) and an allocated coding quantity (T) of a MB (macro block) to determine the quantization step size (See Katata, Col. 3 line 46-58). Furthermore, Katata discloses a virtual buffer for each picture type (See Katata Col. 4, lines 10-12) and that the initial value of the virtual buffer initial is not zero, i.e., a certain constant (See Katata Col. 3, lines 59-61). In addition, the assigned allocation coding quantity (T) derived from the virtual buffer is also provided for each picture type, but is not constant (See Katata Col. 3, lines 15-24).

Based on the foregoing, and contrary to the Examiner's allegation, the Applicant respectfully submits that Katata's virtual buffer fullness simply does not indicate the bit balance of the generated code quantity (B) with respect to the average code bit rate. Katata is clearly deficient in adjusting the quantization step size based on the bit balance of the generated bit count with respect to the average bit rate as recited in Claims 1, 11 and 21. The columns in Katata cited by the Examiner in the response to arguments section do not rectify the foregoing deficiency. More specifically, in Cols. 1 and 2, Katata merely disclose bit allocation, not adjustment of the reference quantization step size. Further, in Cols. 3 and 4, Katata discloses setting the reference quantization step size and adjusting the reference quantization step size. However, whereas the claimed invention adjusts the quantization step size based on the bit balance of the generated bit



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count with respect to the average bit rate, Katata adjusts the quantization step size based on a generated code quantity (B) and an allocated coding quantity (T) of a MB (macro block). Consequently, the Applicant respectfully submits that Katata does not disclose adjusting the quantization step size for each second image unit based on the bit balance of the generated code bit count with respect to the average code bit rate, as particularly recited in Claims 1, 11 and 21.

In view of the foregoing, the Applicant respectfully requests the Examiner to withdraw the rejections of independent Claim 1, 11 and 21 pursuant to 35 U.S.C. §102(b). Furthermore, Applicant respectfully requests the Examiner to withdraw the rejections of dependent Claims 2-10 and 2-20 pursuant to 35 U.S.C. §102(b), based on their respective dependencies from independent Claims 1 and 11, respectively.

In view of the foregoing, the Applicant believes that the above-identified application is in condition for allowance and henceforth respectfully solicits the allowance of the application. If the Examiner believes a telephone conference might expedite the allowance of this application, Applicant respectfully requests that the Examiner call the undersigned, Applicant's attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,

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